ABSTRACT OF THE DISCLOSURE

A plurality of non volatile memory cells, for example of the flash type, with low circuit area occupation, are organized in cell matrices with corresponding circuits responsible for addressing, decoding, reading, writing and erasing the memory cell content. Each of the cells has a gate terminal biased in the programming phase with a predetermined voltage value through operation of charge pump voltage regulators. A first and a second regulation stage, which are structurally independent, are responsible for the programming and soft programming phase respectively. The first stage generates a supply voltage for the second stage.